In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-13. (Canceled).

14. (previously presented) An ~~an~~ integrated circuit chip package comprising:

an integrated circuit chip attached to a substrate;

a stress buffering material only covering corners of said integrated circuit chip; and

an encapsulation material coating said integrated circuit chip and a portion of said substrate.

15. (Original) The package according to claim 14 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

16. (Original) The package according to claim 14 wherein said integrated circuit chip is attached to said substrate by a super ball grid array(SBGA) like structure.

17. (currently amended) The package according to claim 14 wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at said corners ~~at least one corner~~ of said integrated circuit chip.

18. (Original) The package according to claim 14 wherein said stress buffering material comprises an epoxy or resin.

19. (Original) The package according to claim 14 wherein said stress buffering material has a low coefficient of thermal expansion.

20. (Original) The package according to claim 21 wherein said integrated circuit chip contains low dielectric constant dielectric layers.

21. (currently amended) An integrated circuit chip package comprising:

~~A die;~~

an integrated circuit chip having a first surface and a second surface opposite thereto, wherein said second surface is attached to a substrate;

a stress buffering material having a substantially equal ~~similar~~ coefficient of thermal expansion to ~~with~~ said integrated circuit chip ~~die~~, covering at least one corner of said integrated circuit chip ~~die~~ ,wherein a part of the first surface is not covered by the stress buffering material; and

an encapsulation material covering said integrated circuit chip ~~die~~ and said stress buffering material.

22. (previously presented) The package according to claim 21 wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at least one corners of said integrated circuit chip ~~die~~.

23. (previously presented) The package according to claim 21 wherein said stress buffering material comprises an epoxy or resin.

24. (previously presented) The package according to claim 21 wherein said stress buffering material has a low coefficient of thermal expansion.

25. (previously presented) The package according to claim 21 wherein said integrated circuit chip ~~die~~ contains low dielectric constant dielectric layers.

26. (new) The package according to claim 21 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

27. (new) The package according to claim 21 wherein said integrated circuit chip is attached to said substrate by a super ball grid array (SBGA) like structure.